AP 2100

DOCKET NO. P04761 **PATENT**
CLIENT NO. NATI15-04761
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	John E. Gavlik, et al.
Serial No.:	09/713,389
Filed:	November 15, 2000
For:	NETWORK INTERFACE CARD USING PHYSICAL LAYER MICROCONTROLLER AND METHOD OF OPERATION
Group No.:	2157
Examiner:	Hussein A. El-chanti

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

The Appellants have appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner dated August 13, 2004, finally rejecting Claims 1-23. The Appellants filed a Notice of Appeal on February 2, 2005, which was received by the U.S. Patent and Trademark Office on February 7, 2005. The Appellants respectfully submit this brief on appeal with the appropriate statutory fee.

REAL PARTY IN INTEREST

This application is currently owned by National Semiconductor Corporation as indicated by an assignment recorded on November 15, 2000 in the Assignment Records of the United States Patent and Trademark Office at Reel 011331, Frame 0386.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-23 have been rejected pursuant to a final Office Action dated August 13, 2004. Claims 1-23 are presented for appeal. A copy of Claims 1-23 is provided in the Appendix.

STATUS OF AMENDMENTS

An AMENDMENT AND RESPONSE TO OFFICE ACTION was filed on October 12, 2004. In an Advisory Action dated March 9, 2005, the Examiner refused to enter the AMENDMENT AND RESPONSE, stating it did not place the application in condition for allowance.

SUMMARY OF CLAIMED SUBJECT MATTER

Regarding Claim 1, an apparatus for controlling a physical layer interface of a network interface card 140 includes a read only memory 260 or 320, a random access memory 270 or 330, and a microcontroller 300. (*Application, Figure 3; Page 15, Line 14 – Page 16, Line 3*). The read only memory 260 or 320 is capable of storing an embedded control program. (*Application, Page 17, Lines 5-22; Page 5, Lines 7-8 and 18-19; Page 6, Lines 1-3*). The random access memory 270 or 330 is capable of storing a downloadable software control program. (*Application, Page 18, Lines 1-6; Page 5, Lines 8-9 and 20-21; Page 6, Lines 4-5*). The microcontroller 300, in a first operating mode, executes the embedded control program to control the physical layer interface. (*Application, Page 17, Lines 5-9; Page 5, Lines 9-13*). The microcontroller 300, in a second operating mode, is capable of downloading the downloadable software control program from an external processing system and executing the software control program in place of the embedded control program to control the physical layer interface. (*Application, Page 18, Lines 2-6; Page 5, Lines 13-17*).

Regarding Claim 9, a processing system 100 includes a data processor 106. (*Application, Page 11, Lines 9-16*). The processing system 100 also includes a hard disk drive 103 that is capable of storing a network interface card configuration file 150 containing a downloadable software control program. (*Application, Figure 1; Page 12, Lines 17-22*). In addition, the processing system 100 includes a network interface card 140 for coupling the processing system 100 to a data network. (*Application, Page 12, Lines 12-13*). The network interface card 140 includes an apparatus for controlling a physical layer interface of the network interface card 140. (*Application, Page 12, Line 19 – Page 13, Line 8*). The apparatus includes a read only memory 260 or 320, a random access

memory 270 or 330, and a microcontroller 300. (*Application, Figure 3; Page 15, Line 14 – Page 16, Line 3*). The read only memory 260 or 320 is capable of storing an embedded control program. (*Application, Page 17, Lines 5-22; Page 5, Lines 7-8 and 18-19; Page 6, Lines 1-3*). The random access memory 270 or 330 is capable of storing the downloadable software control program. (*Application, Page 18, Lines 1-6; Page 5, Lines 8-9 and 20-21; Page 6, Lines 4-5*). The microcontroller 300, in a first operating mode, executes the embedded control program to control the physical layer interface. (*Application, Page 17, Lines 5-9; Page 5, Lines 9-13*). The microcontroller 300, in a second operating mode, is capable of downloading the downloadable software control program from an external processing system and executing the software control program in place of the embedded control program to control the physical layer interface. (*Application, Page 18, Lines 2-6; Page 5, Lines 13-17*).

Regarding Claim 17, a method of operating a microcontroller 300 for controlling a physical layer interface in a network interface card 140 is provided. In a first operating mode, an embedded control program stored in a read only memory 260 or 320 is executed to control the physical layer interface. (*Application, Page 17, Lines 5-9; Page 5, Lines 9-13*). In a second operating mode, a software control program is downloaded from an external processing system and stored in a random access memory 270 or 330. (*Application, Page 18, Lines 2-6; Page 5, Lines 13-15*). In response to the step of downloading the software control program, the software control program is executed in place of the embedded control program to control the physical layer interface. (*Application, Page 5, Lines 13-17*).

GROUNDS OF REJECTION

1. Claims 1-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,856,975 to Rostoker et al. ("*Rostoker*").

ARGUMENT

I. GROUND OF REJECTION #1

The rejection of Claims 1-23 under 35 U.S.C. § 102(b) is improper and should be withdrawn.

A. OVERVIEW

Claims 1-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,856,975 to Rostoker et al. ("*Rostoker*").

B. STANDARD

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

C. THE *ROSTOKER* REFERENCE

Rostoker recites a high speed digital video network apparatus that is implemented on a single integrated circuit chip. (*Abstract*). One embodiment of the digital video network apparatus 300 includes network protocol processing system interconnection circuits 323. (*Col. 8, Lines 37-41*). The interconnection circuits 323 may include circuits such as a physical layer interface unit 332, a network protocol processing unit 333, a random access memory (RAM) 334, and a serial programmable read only memory (PROM) 336. (*Figure 3; Col. 9, Lines 29-43*).

The interconnection circuits 323 are shown in more detail in Figure 16 of *Rostoker*. (*Col. 23, Lines 41-42*). As shown in Figure 16, the network protocol processing unit 333 includes elements such as an ATM processor unit (APU) 500, a virtual channel RAM (VCR) 501, a direct memory access (DMA) controller 502, and an instruction RAM (IRAM) 506. (*Col. 23, Lines 43-59*). The APU 500 implements various functions related to communication over a network using Asynchronous Transfer Mode (ATM) cells. (*Col. 24, Lines 1-19*). The APU 500 could represent a reduced instruction set computer (RISC) processing unit. (*Col. 24, Lines 2-7*). The APU 500 executes software stored in the IRAM 506, and the software may be loaded into the IRAM 506 upon a system reset or otherwise downloaded into the IRAM 506. (*Col. 24, Lines 20-27; Col. 23, Lines 63-65*). The DMA controller 502 controls the transfer of data, such as transfers between the VCR 501 and memory mapped devices. (*Col. 25, Lines 3-6*).

D. CLAIMS 1-7, 9-15, AND 17-23

Claim 1 recites an apparatus for controlling a physical layer interface of a network interface

card, which includes:

> a read only memory (ROM) capable of storing an embedded control program;
>
> a random access memory capable of storing a downloadable software control program; and
>
> a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said embedded control program to thereby control said physical layer interface.

In order to properly reject Claim 1, the Examiner must show that *Rostoker* anticipates a "microcontroller" that executes an "embedded control program" in a "first operating mode" and that executes a "downloadable software control program" in a "second operating mode," where the "embedded control program" is stored in a read only memory and the "downloadable software control program" is stored in a random access memory. The Examiner must also show that *Rostoker* executes the downloadable software control program "in place of" the embedded control program when in the "second operating mode."

The Examiner fails to make these showings. In particular, the Examiner fails to show that *Rostoker* anticipates executing different "control programs" in different "operating modes" to control a "physical layer interface." The Examiner also fails to show that *Rostoker* anticipates executing a downloadable control program "in place of" an embedded control program.

The Examiner relies on two portions of *Rostoker* as anticipating the read only memory recited in Claim 1. (*08/13/04 Office Action, Page 2, Section 2, Third paragraph*). The first portion (column

9, lines 31-40) recites the use of a programmable read only memory (PROM) 336. The second portion (column 28, lines 55-65) recites that an "address sourcing capability" for direct memory access may be used to "boot from a ROM or other device." The Examiner relies on the IRAM (such as IRAM 506) of *Rostoker* as anticipating the "random access memory" recited in Claim 1. (*08/13/04 Office Action, Page 2, Section 2, Fourth paragraph*).

Based on these assertions, the Examiner must prove that a "microcontroller" in *Rostoker* executes a "control program" stored in one of the ROMs during a "first operating mode" and executes a different "control program" stored in the IRAM 506 during a "second operating mode." The Examiner must also prove that a control program stored in the IRAM 506 is executed "in place of" a control program stored in one of the ROMs to control a "physical layer interface."

First, the Examiner has not shown that a first "control program" is stored in the PROM 336 and executed during a "first operating mode" and that a second "control program" is stored in the IRAM 506 and executed during a "second operating mode." The Examiner cites no portion of *Rostoker* showing that the interconnection circuits 323 of *Rostoker* execute instructions from the PROM 336 in a "first operating mode" and instructions from the IRAM 506 in a "second operating mode." *Rostoker* simply recites that software is loaded into the IRAM 506 and executed by the APU 500. *Rostoker* lacks any mention that instructions in the PROM 336 are only executed in a first "mode" and that the software in the IRAM 506 is only executed in a second "mode."

Moreover, assume (without admitting) that the PROM 336 of *Rostoker* stores a control program. The Examiner has not established that a different control program from the IRAM 506 is executed "in place of" the control program in the PROM 336 when in the "second operating mode."

The Examiner cites no portion of *Rostoker* showing that the interconnection circuits 323 execute instructions from the PROM 336 in one mode and then switch to executing instructions from the IRAM 506 in another mode. The Examiner also cited no portion of *Rostoker* showing that the instructions in the IRAM 506 are used to replace instructions in the PROM 336. In fact, *Rostoker* lacks any mention of executing instructions in the IRAM 506 "in place of" the instructions in the PROM 336

As a result, the Examiner has not established that executing the contents of the PROM 336 and IRAM 506 anticipates executing an "embedded control program" in a "first operating mode" and a "downloadable software control program" in a "second operating mode," where the "embedded control program" is stored in a read only memory and the "downloadable software control program" is stored in a random access memory as recited in Claim 1. The Examiner also has not shown that executing the contents of the PROM 336 and IRAM 506 anticipates executing a downloadable software control program "in place of" an embedded control program when in the "second operating mode" as recited in Claim 1.

Second, regarding the ROM referenced in column 28, lines 55-65 of *Rostoker* (referred to here as a "boot ROM"), the Examiner has not shown that a first "control program" for controlling a "physical layer interface" is stored in the boot ROM and executed during a "first operating mode." The Examiner also has not shown that a different control program in the IRAM 506 of *Rostoker* is executed during a "second operating mode" and that the program in the IRAM 506 is executed "in place of" a program in the boot ROM to control the "physical layer interface."

The cited portion of *Rostoker* simply refers to the fact that an "address sourcing capability"

for direct memory access could be used to boot from the boot ROM. This portion of *Rostoker* lacks any mention of storing an "embedded control program" used to control a "physical layer interface" in the boot ROM. This portion of *Rostoker* also lacks any mention of executing a different control program "in place of" a program stored in the boot ROM. Instead, this portion of *Rostoker* simply indicates that different signals may need to be asserted or deasserted to avoid problems during initialization of the network protocol processing unit 333. (*Col. 28, Lines 59-65*).

As a result, the Examiner has not established that executing the contents of the boot ROM and the IRAM 506 anticipates executing an "embedded control program" in a "first operating mode" and a "downloadable software control program" in a "second operating mode," where the "embedded control program" is stored in a read only memory and the "downloadable software control program" is stored in a random access memory as recited in Claim 1. The Examiner also has not shown that executing the contents of the boot ROM and IRAM 506 anticipates executing a downloadable software control program "in place of" an embedded control program when in the "second operating mode" as recited in Claim 1.

Third, the Examiner mischaracterizes Claim 1 in the Advisory Action dated March 9, 2005. In the Advisory Action, the Examiner states that *Rostoker* downloads a control program into an IRAM in "write mode" and then executes the control program in a "processing mode." (*03/09/05 Advisory Action, Page 2, First paragraph*). Based on this, the Examiner states that *Rostoker* anticipates "downloading a control program in a first mode and executing the control program in a second mode." (*03/09/05 Advisory Action, Page 2, First paragraph*).

Claim 1 does not recite downloading a control program in one mode and executing the same

control program in another mode. Claim 1 recites that different control programs are executed in different modes. More specifically, Claim 1 recites that an "embedded control program" is executed in a "first operating mode" and a "downloadable software control program" is executed in a "second operating mode."

Because of this, the Examiner cannot show that *Rostoker* anticipates Claim 1 by showing that *Rostoker* downloads a control program in one mode and executes the same control program in another mode. Rather, the Examiner must show that *Rostoker* executes an "embedded control program" in one mode and that *Rostoker* executes a "downloadable software control program" in place of the embedded control program in another mode. As shown above, the Examiner has not established that *Rostoker* executes an "embedded control program" to control a "physical layer interface" in one mode and a "downloadable software control program" to control the "physical layer interface" in another mode. The Examiner also has not shown that *Rostoker* executes the "downloadable software control program" to control the physical layer interface "in place of" the "embedded control program."

For these reasons, *Rostoker* fails to anticipate all elements of Claim 1. As a result, Claim 1 and its dependent claims are patentable over *Rostoker*. *Rostoker* also fails to anticipate analogous elements recited in Claims 9 and 17. As a result, Claims 9 and 17 and their dependent claims are patentable over *Rostoker*.

Accordingly, the Appellants respectfully request that the final rejection of Claims 1-7, 9-15, and 17-23 be withdrawn and that Claims 1-7, 9-15, and 17-23 be passed to allowance.

E. CLAIMS 8 AND 16

Claims 8 and 16 depend from Claims 1 and 9, respectively. Claims 8 and 16 are patentable due to their dependence from patentable base claims and in light of their own recitations. For example, Claim 8 recites that the microcontroller (recited in Claim 1) includes a "plurality of control registers." The microcontroller switches from the first operating mode to the second operating mode when an "external processing system" stores a "jump address" in a first one of the control registers.

The Examiner cites two portions of *Rostoker* as anticipating these elements of Claim 8. The first portion (column 28, lines 46-65) recites how software is stored in the IRAM 506. In particular, this portion of *Rostoker* recites how various control signals (such as "Resetx," "DMA_DataOEx," "DMA_AdrOEx," and "DNA_RdWrAck") are asserted and deasserted.

This portion of *Rostoker* lacks any mention of using multiple "control registers." This portion of *Rostoker* also lacks any mention of storing a "jump address" in a register, where the jump address causes a microprocessor to change "operating modes" and begin executing one control program "in place of" another control program. As a result, this portion of *Rostoker* fails to anticipate Claim 8.

The second portion (column 29, line 54 – column 30, line 8) of *Rostoker* recites how the APU 500 processes ATM cells stored in the virtual channel RAM (VCR) 501. (*Col. 29, Lines 57-67*). This portion of *Rostoker* also recites the use of "memory pointers" for the VCR 501. (*Col. 30, Lines 7-8*).

Once again, this portion of *Rostoker* lacks any mention of storing a "jump address" in a "control register." This portion of *Rostoker* also lacks any mention that the jump address causes a

microprocessor to change "operating modes" and begin executing one control program "in place of" another control program. As a result, this portion of *Rostoker* also fails to anticipate Claim 8.

For these reasons, *Rostoker* fails to anticipate all elements of Claim 8. As a result, Claim 8 is patentable over *Rostoker*. *Rostoker* also fails to anticipate analogous elements recited in Claim16. As a result, Claim 16 is patentable over *Rostoker*.

Accordingly, the Appellants respectfully request that the final rejection of Claims 8 and 16 be withdrawn and that Claims 8 and 16 be passed to allowance.

SUMMARY

The Appellants have demonstrated that the present invention as claimed is clearly distinguishable over the prior art cited of record. Therefore, the Appellants respectfully request the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

The Appellants have enclosed the appropriate fee to cover the cost of this APPEAL BRIEF. The Appellants do not believe that any additional fees are due. However, the Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) or credit any overpayments to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: April 7, 2005

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APPENDIX

PENDING CLAIMS

1. An apparatus for controlling a physical layer interface of a network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program;

a random access memory capable of storing a downloadable software control program; and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said embedded control program to thereby control said physical layer interface.

2. The apparatus as set forth in Claim 1 wherein said ROM is an internal ROM in said microcontroller.

3. The apparatus as set forth in Claim 1 wherein said RAM is an internal RAM in said microcontroller.

4. The apparatus as set forth in Claim 1 wherein said ROM is an external ROM coupled to said microcontroller.

5. The apparatus as set forth in Claim 1 wherein said RAM is an external RAM coupled to said microcontroller.

6. The apparatus as set forth in Claim 1 wherein said microcontroller downloads said downloadable software control program from said external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

7. The apparatus as set forth in Claim 6 wherein said microcontroller downloads said downloadable software control program via a medium access control (MAC) layer interface coupling said external processing system and said physical layer interface.

8. The apparatus as set forth in Claim 1 wherein said microcontroller further comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address in said RAM in a first one of said plurality of control registers.

9. A processing system comprising:

a data processor;

a hard disk drive capable of storing thereon a network interface card (NIC) configuration file containing a downloadable software control program; and

a network interface card for coupling said processing system to a data network, said network interface card comprising:

an apparatus for controlling a physical layer interface of said network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program;

a random access memory capable of storing a downloadable software control program; and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said embedded control program to thereby control said physical layer interface.

10. The processing system as set forth in Claim 9 wherein said ROM is an internal ROM in said microcontroller.

11. The processing system as set forth in Claim 9 wherein said RAM is an internal RAM in said microcontroller.

12. The processing system as set forth in Claim 9 wherein said ROM is an external ROM coupled to said microcontroller.

13. The processing system as set forth in Claim 9 wherein said RAM is an external RAM coupled to said microcontroller.

14. The processing system as set forth in Claim 9 wherein said microcontroller downloads said downloadable software control program from said external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

15. The processing system as set forth in Claim 14 wherein said microcontroller downloads said downloadable software control program via a medium access control (MAC) layer interface coupling said external processing system and said physical layer interface.

16. The processing system as set forth in Claim 9 wherein said microcontroller further comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address in said RAM in a first one of said plurality of control registers.

17. For use in a network interface card having a physical layer interface controllable by a microcontroller embedded therein, a method of operating the microcontroller comprising the steps of:

in a first operating mode, executing an embedded control program stored in a read only memory (ROM) coupled to the microcontroller to thereby control the physical layer interface; and

in a second operating mode, downloading a software control program from an external processing system and storing the software control program in a random access memory (RAM) coupled to the microcontroller and, in response to the step of downloading the software control program, executing the software control program in place of the embedded control program to thereby control the physical layer interface.

18. The method as set forth in Claim 17 wherein the ROM is an internal ROM in the microcontroller.

19. The method as set forth in Claim 17 wherein the RAM is an internal RAM in the microcontroller.

20. The method as set forth in Claim 17 wherein the ROM is an external ROM coupled to the microcontroller.

21. The method as set forth in Claim 17 wherein the RAM is an external RAM coupled to the microcontroller.

22. The method as set forth in Claim 17 wherein the step of downloading comprises the step of downloading the software control program from the external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

23. The method as set forth in Claim 22 wherein the step of downloading comprises the step of downloading the software control program via a medium access control (MAC) layer interface coupling the external processing system and the physical layer interface.

DOCKET NO. P04761 **PATENT**
CLIENT NO.: NATI15-04761
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	JOHN E. GAVLIK, ET AL.
U.S. Serial No.	:	09/713,389
Filed	:	November 15, 2000
For	:	NETWORK INTERFACE CARD USING PHYSICAL LAYER MICROCONTROLLER AND METHOD OF OPERATION
Group No.	:	2157
Examiner	:	Hussein A. El-chanti

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Appeal Brief;
2. Check in the amount of $500.00 for the Appeal Brief Filing Fee;
3. Fee Transmittal for FY 2005 (in duplicate); and
4. A postcard receipt

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 7, 2005.

Date: April 7, 2005 Kathy Hamilton
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PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/713,389
Filing Date	November 15, 2000
First Named Inventor	John E. Gavlik
Examiner Name	Hussein A. El-chanti
Art Unit	2157
Attorney Docket No.	P04761 (NATI15-04761)

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: DAVIS MUNCK, P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Appeal Brief Fee	$500.00

SUBMITTED BY

Signature	William A. Munck	Registration No. (Attorney/Agent) 39,308	Telephone 972-628-3600
Name (Print/Type)	William A. Munck		Date April 7, 2005